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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,886	07/11/2003	James W. Cady	254-094-CIP-5	1819
36485	7590	10/05/2005	EXAMINER	
J. SCOTT DENKO ANDREWS & KURTH LLP 111 CONGRESS AVE., SUITE 1700 AUSTIN, TX 78701			VIGUSHIN, JOHN B	
			ART UNIT	PAPER NUMBER
			2841	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/631,886

Applicant(s)

CADY ET AL.

Examiner

John B. Vigushin

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1,2 and 25-27 is/are allowed.
- 6) ☒ Claim(s) 3,6,8,23,24 and 28-33 is/are rejected.
- 7) ☒ Claim(s) 4,5,7,9-22,34 and 35 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date see "Other" box #6.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: See Continuation Sheet.

Continuation of Attachment(s) 6). Other: The following IDS (PTO-1449) papers were submitted by the Applicant and reviewed and signed by the Examiner: 0805a//15 Aug 2005 (8 sheets); 0805b//15 Aug 2005 (3 sheets); 0805c (1 sheet); 0105//07 Jan 2005 (2 sheets); 0404 (1 sheet); 0204//09 Feb 2004 (9 sheets)..

DETAILED ACTION

Specification (Abstract)

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet **within the range of 50 to 150 words**. **It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited.** The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. **The abstract of the disclosure is objected to because it exceeds 150 words in length.** Correction is required. See MPEP § 608.01(b).

Rejections Based On Prior Art

3. The following references were relied upon for the rejections hereinbelow:

Warner et al. (US 2003/0168725 A1)*

Isaak (6,323,060 B1)**

Damberg (US 6,765,288 B2)

*Made of record in Applicant's IDS, filed August 15, 2005.

**Made of record in Applicant's IDS, filed April 13, 2004.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 24 and 28-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Isaak [Examiner's Note: Isaak (patent date: November 27, 2001) qualifies as § 102(b) prior art because Claims 24 and 28-30 claim combinations of limitations that include the new matter of the instant CIP Application which was filed July 11, 2003].

As to Claim 24, Isaak discloses: a first CSP 104 (the upper CSP 104 in Fig. 28; col.4: 6-14); flex circuitry 102; and a second CSP 104 (the lower CSP 104 in Fig. 28) in a stacked relationship with the first CSP 104, the second CSP having plural consolidated contacts 106, each of which is one piece of metal that has been melted to pass in part through the flex circuitry 102 to provide a connection between the second CSP 104 and the flex circuitry 102 and a module connective facility (col.9: 59-col.10: 4).

As to Claim 28, Isaak discloses: providing a first CSP 104 (the lower CSP 104 in Fig. 28; col.4: 6-14) having a plurality of ball contacts 106 disposed along a major surface (Fig. 21; col.10: 7-9); providing flex circuitry 102 having a plurality of selected flex contacts 112, each penetrated by an orifice 118 (Fig. 20; col.9: 41-54); disposing the first CSP 104 proximal to the flex circuitry 102 to place the plurality of ball contacts adjacent to the plurality of flex contacts 112 (col.9: 59-67); applying heat sufficient to

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melt the plurality of ball contacts (in the case that the ball contacts 106 are coated with flux, then the ball contacts are melted; col.10: 1-4).

As to Claim 29, Isaak further discloses disposing a second CSP 104 above the first CSP 104 and connecting the first and second CSPs 104 with the flex circuitry 102 (Fig. 28; col.10: 45-61).

As to Claim 30, Isaak further discloses the flex circuitry is comprised of two flex circuits 102 (Figs. 27 and 28; one flex circuit 102 on the lower package, and the other flex circuit 102 on the upper package, electrically connected by conductive adhesive 150; col.10: 45-54).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

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consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 23, 24, 28, 29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Warner et al. in view of Isaak.

A) As to Claim 23:

I. Warner et al. discloses: a first microelectronic package 101d; a second microelectronic package 101c, the second microelectronic package 101c disposed above the first microelectronic package 101d (Fig. 3A; paragraph [0043]); flex circuitry 110 (paragraph [0044]) connecting the first microelectronic package 101d and the second microelectronic package 101c, the flex circuitry 110 having plural flex contacts 117 of which at least one has an orifice that has a median opening extent of DO (Fig. 3D; last five lines of paragraph [0046]); plural consolidated contacts 108, a selected one of which passes through the orifice (Fig. 3D) and the selected one of the plural consolidated contacts 108 having an inner flex portion (adjacent microelectronic package 101d) and an outer flex portion delineated by the orifice (Fig. 3D), the selected one of the plural consolidated contacts 108 providing a connection between the first microelectronic package 101d (at pad 103 of package 101d) and the flex circuitry (at pad or via metallization 117; last five lines of paragraph [0046]) and the outer flex of consolidated contact 108 having a median lateral extent of DCC and DCC is larger than DO (Fig. 3D).

II. Warner et al. discloses microelectronic packages 101a,b,c,d flip-chip mounted to flex circuitry 110 (paragraph [0044]) but does not disclose packages 101a,b,c,d of a

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specific type; e.g., chip scale packages. However, Warner et al. further discloses that the microelectronic packages may include a wide variety of chips and packaged chips (paragraph [0042]).

III. Isaak discloses an IC device 104 flip-chip mounted to flex circuitry 102 (Figs. 22 and 25) and arranged in stacked assembly (Fig. 28). Isaak further discloses that the IC device 104 may any one of several types of IC devices including a chip scale package (CSP) (col.4: 1-14).

IV. Since both Warner et al. and Isaak are both in the art of stacked packaging of IC devices by means of flex circuitry and since Isaak discloses that among the packaged devices that can be stacked in such a manner are CSPs, then the use of CSPs, as taught by Isaak, as the microelectronic packages stacked by means of flex circuitry, in Warner et al., would have been readily recognized as one of the wide variety of IC packages that may be so assembled, as clearly taught in paragraph [0042] in the pertinent art of Warner et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the stacked package assembly of Warner et al. using CSPs as the microelectronic package devices, as taught by Isaak, in order to enhance the functionality of the stacked package of Warner et al. with the high circuit density and compact dimensions of CSPs, as in Isaak.

B) As to Claim 24:

I. Warner et al. discloses a first microelectronic device 101c (Fig. 3A; paragraph [0043]); flex circuitry 110 (paragraph [0044]); a second microelectronic device 101d in

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stacked relationship with first microelectronic device 101c (Fig. 3A), the second microelectronic device 101d having plural consolidated contacts 108 (Fig. 3D) each of which is one piece of metal (solder; see paragraph [0045]) that has been melted to pass in part through the flex circuitry to provide a connection between the second microelectronic device 101d and the flex circuitry 110 and a module connective facility (paragraph [0045] and last five lines of paragraph [0046]).

II. Warner et al. discloses microelectronic packages 101a,b,c,d flip-chip mounted to flex circuitry 110 (paragraph [0044]) but does not disclose packages 101a,b,c,d of a specific type; e.g., chip scale packages. However, Warner et al. further discloses that the microelectronic packages may include a wide variety of chips and packaged chips (paragraph [0042]).

III. Isaak discloses an IC device 104 flip-chip mounted to flex circuitry 102 (Figs. 22 and 25) and arranged in stacked assembly (Fig. 28). Isaak further discloses that the IC device 104 may any one of several types of IC devices including a chip scale package (CSP) (col.4: 1-14).

IV. Since both Warner et al. and Isaak are both in the art of stacked packaging of IC devices by means of flex circuitry and since Isaak discloses that among the packaged devices that can be stacked in such a manner are CSPs, then the use of CSPs, as taught by Isaak, as the microelectronic packages stacked by means of flex circuitry, in Warner et al., would have been readily recognized as one of the wide variety of IC packages that may be so assembled, as clearly taught in paragraph [0042] in the pertinent art of Warner et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the stacked package assembly of Warner et al. using CSPs as the microelectronic package devices, as taught by Isaak, in order to enhance the functionality of the stacked package of Warner et al. with the high circuit density and compact dimensions of CSPs, as in Isaak.

C) As to Claim 28:

I. Warner et al. discloses providing a first microelectronic device 101d having a plurality of ball contacts 108 disposed along a major surface (Figs. 3A and 3D; first two lines of paragraph [0044]); providing flex circuitry 110 (paragraph [0044]) having a plurality of selected flex contacts 117, each penetrated by an orifice (Fig. 3D; first six lines and last five lines of paragraph [0046]); disposing the first microelectronic device 101d proximal to the flex circuitry 110 to place the plurality of ball contacts adjacent to the plurality of flex contacts 117 (Figs. 3A and 3D; paragraph [0044]); applying heat sufficient to melt the plurality of ball contacts (paragraph [0045] teaches that the ball contacts may comprise solder, among other bonding materials, and inherently, the step of heating the solder would be required for the ball contacts 108 to penetrate the orifice, as shown in Fig. 3D).

II. Warner et al. discloses microelectronic packages 101a,b,c,d flip-chip mounted to flex circuitry 110 (paragraph [0044]) but does not disclose packages 101a,b,c,d of a specific type; e.g., chip scale packages. However, Warner et al. further discloses that the microelectronic packages may include a wide variety of chips and packaged chips (paragraph [0042]).

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III. Isaak discloses an IC device 104 flip-chip mounted to flex circuitry 102 (Figs. 22 and 25) and arranged in stacked assembly (Fig. 28). Isaak further discloses that the IC device 104 may any one of several types of IC devices including a chip scale package (CSP) (col.4: 1-14).

IV. Since both Warner et al. and Isaak are both in the art of stacked packaging of IC devices by means of flex circuitry and since Isaak discloses that among the packaged devices that can be stacked in such a manner are CSPs, then the use of CSPs, as taught by Isaak, as the microelectronic packages stacked by means of flex circuitry, in Warner et al., would have been readily recognized as one of the wide variety of IC packages that may be so assembled, as clearly taught in paragraph [0042] in the pertinent art of Warner et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the stacked package assembly of Warner et al. using CSPs as the microelectronic package devices, as taught by Isaak, in order to enhance the functionality of the stacked package of Warner et al. with the high circuit density and compact dimensions of CSPs, as in Isaak.

D) As to Claim 29, modified Warner et al. further discloses the step of disposing a second microelectronic device (CSP) 101c above first microelectronic device (CSP) 101d (Fig. 3A) and connecting the first and second CSPs with the flex circuitry 110 (Fig. 1 shows the wiring 115 that interconnects the mounting sites 113; see paragraph [0040]).

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E) As to Claim 31, modified Warner et al. further discloses that the flex circuitry 110 has two conductive layers (one conductive layer on surface 111, as in Fig. 1, and one conductive layer on surface 112, as in Fig. 2; see paragraph [0040]).

9. Claims 3, 6, 8, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Damberg in view of Isaak.

A) As to Claim 3:

I. Damberg discloses: a first microelectronic device 644 (Fig. 12) having an upper surface and a lower surface and a body with a height H1, and along the lower surface there are plural first device low profile contacts (consisting of 658, 602, 634 and 630; see Figs. 12 and 13), each of which extends no more than 7 mils from the surface (col.11: 46-col.12: 6, wherein shortest of the range of heights h1 and h2 given in microns adds up to $140\text{ }\mu\text{m} = 5.5\text{ mils}$); a second microelectronic device (Fig. 12; i.e., device 60 or 78, as in Fig. 4) in stacked disposition with the first microelectronic device 644, the second microelectronic device having an upper surface and a lower surface and a body with a height H2, and along the lower surface there are plural second device low profile contacts (in flex circuit portion 628), each of which extends no more than 7 mils from the surface of the second microelectronic device (Fig. 12); a first flex circuitry 620 that connects first microelectronic device 644 with the second microelectronic device, a portion 628 of which flex circuitry is disposed between the first and second microelectronic devices (Fig. 12).

II. Damberg discloses that the first and second microelectronic devices may be packaged devices, such as memory devices (col.5: 50-55; col.7: 41-53) or other types

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of devices (col.13: 18-30). Damberg does not teach that the first and second microelectronic devices are chip scale packages (CSP).

III. Isaak discloses an IC device 104 flip-chip mounted to flex circuitry 102 (Figs. 22 and 25) and arranged in stacked assembly (Fig. 28). Isaak further discloses that the IC device 104 may any one of several types of IC devices including a chip scale package (CSP) (col.4: 1-14) used as memory devices (col.1: 10-19).

IV. Since both Damberg and Isaak are both in the art of stacked packaging of IC devices by means of flex circuitry and since Isaak discloses that among the packaged memory devices that can be stacked in such a manner are CSPs, then the use of CSP memory devices, as taught by Isaak, as the microelectronic devices stacked by means of flex circuitry, in Damberg, would have been readily recognized as an application of CSPs for the memory devices in the stacked assembly of the pertinent art of Damberg.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the stacked package assembly of Damberg using CSP memory devices as the microelectronic package devices, as taught by Isaak, in order to enhance the functionality of the stacked package of Warner et al. with the high circuit density and compact dimensions of CSPs, as in Isaak.

B) As to Claims 6 and 8, modified Damberg further discloses the shortest distance from the lower surface of the second CSP to the upper surface of first CSP 644 is less than 11 mils and no more than 9 mils (Fig. 12; col.12: 1-6).

C) As to Claim 32:

I. Damberg discloses: providing a first microelectronic device 644 having contact sites 658 along a major surface (Fig. 13); providing a second microelectronic device having contact sites along a major surface (sites 58, as in the second microelectronic devices in Figs. 4 and 5); providing flex circuitry 620 having plural flex contacts 634 (Fig. 13); disposing solder 662 (col.11: 50-52) to selected contact sites of first microelectronic device 644 to a first set of the plural flex contacts 634 so that the shortest distance from the major surface 650 of first microelectronic device 644 to a surface 622 of the flex circuitry 620 is between 1 and 6 mils inclusive (said "shortest distance" is $h1 = 40$ to $50 \mu\text{m}$ which is 1.6 to 1.9 mils; col.11: 46-50).

II. Damberg discloses that the first and second microelectronic devices may be packaged devices, such as memory devices (col.5: 50-55; col.7: 41-53) or other types of devices (col.13: 18-30). Damberg does not teach that the first and second microelectronic devices are chip scale packages (CSP).

III. Isaak discloses an IC device 104 flip-chip mounted to flex circuitry 102 (Figs. 22 and 25) and arranged in stacked assembly (Fig. 28). Isaak further discloses that the IC device 104 may any one of several types of IC devices including a chip scale package (CSP) (col.4: 1-14) used as memory devices (col.1: 10-19).

IV. Since both Damberg and Isaak are both in the art of stacked packaging of IC devices by means of flex circuitry and since Isaak discloses that among the packaged memory devices that can be stacked in such a manner are CSPs, then the use of CSP memory devices, as taught by Isaak, as the microelectronic devices stacked by means

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of flex circuitry, in Damberg, would have been readily recognized as an application of CSPs for the memory devices in the stacked assembly of the pertinent art of Damberg.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the stacked package assembly of Damberg using CSP memory devices as the microelectronic package devices, as taught by Isaak, in order to enhance the functionality of the stacked package of Warner et al. with the high circuit density and compact dimensions of CSPs, as in Isaak.

D) As to Claim 33, modified Damberg further discloses disposing solder to connect selected contact sites of the second CSP to a second set of the plural flex contacts (in flex portion 628) so that the shortest distance from the major surface of the second CSP to a surface of the flex circuitry on flex portion 628 is between 1 and 6 mils (Fig. 12; col.12: 1-6).

Allowable Subject Matter

10. Claims 1, 2 and 25-27 have been allowed.

11. Claims 4, 5, 7, 9-22 and 34-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 1 and 2, patentability resides in *the contacts of the first CSP extending no further than 7 mils above the lower major surface of the first CSP and*

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*being connected to the lower flex contacts of **the first and second flex circuits***, in combination with the other limitations of base Claim 1.

As to Claims 4-5, 7, 9, the reasons for indication of patentability are self-evident.

As to Claims 10 and 12, patentability resides in *a form standard disposed above the upper surface of the first CSP*, in combination with the other limitations of the broadest claim, Claim 10.

As to Claims 11, 13, 14 and 19-22, patentability resides, at least in part, in *a first form standard disposed above the upper surface of the first CSP*, in combination with the other limitations of the broadest claim, Claim 11.

As to Claims 15-18, patentability resides, at least in part, in *a form standard disposed above the upper major surface of the first CSP*, in combination with the other limitations of the broadest claim, Claim 15.

As to Claims 25-27, patentability resides in *a first CSP having a lower surface rising above which lower surface by no more than 7 mils are contacts that are connected to the first flex contacts of each of **the first and second flex circuits***, in combination with the other limitations of base Claim 25.

As to Claims 34-35, patentability resides in the limitation wherein, *the flex circuitry has two conductive layers*, in combination with the other limitations of the broadest claim, Claim 34.

13. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

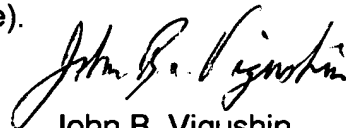
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Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
October 02, 2005